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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/698,550	10/27/2000	Shervin Moloudi	15258US06	5013

23446 7590 12/29/2008
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EXAMINER	
MILORD, MARCEAU	
ART UNIT	PAPER NUMBER
2618	

MAIL DATE	DELIVERY MODE
12/29/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/698,550	MOLOUDI ET AL.	
	Examiner	Art Unit	
	Marceau Milord	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-93* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *33-38 and 70-75* is/are allowed.

6)☒ Claim(s) *1-4,14,32,39-42,61 and 76-93* is/are rejected.

7)☒ Claim(s) *5-13,15-31,43-60 and 62-69* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 39, 61, are rejected under 35 U.S.C. 112, first paragraph, because the best mode contemplated by the inventor has not been disclosed. Evidence of concealment of the best mode is based upon the fact that the bandpass circuit is not coupled to the signal input and the differential signal input as claimed in claims 39 and 61.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 32, 39-42, are rejected under 35 U.S.C. 102(b) as being anticipated by Williams (US Patent No 5557642).

Regarding claims 1- 4, 14, 32, Williams discloses a mixer (fig.3), comprising: a track and hold circuit (331 of fig. 3) to track and hold a first signal which is the first mixer (332 of fig. 3) which is also the first mixer in response to a second signal; and a bandpass circuit in cooperation with the track and hold circuit (fig. 3; col. 3, lines 49-56; col. 4, lines 18-65; col. 5, lines 1-50; col. 6, lines 10-42).

Regarding claims 39-42, Williams discloses a mixer (fig. 3) comprising: a control input, and a mixed signal output (fig. 3; col. 3, lines 49-56; col. 4, lines 18-65; col. 5, lines 1-50; col. 6, lines 10-42).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 61, 76-93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lloyd et al (US Patent No 6298226 B1) in view of Williams (US Patent No 5557642).

Regarding claim 61, Dacus et al discloses a differential mixer (figs. 3-6; figs. 7-9) comprising: a track and hold circuit (col. 3, lines 15-31) having a differential signal input, a differential control input, and a differential mixed signal output (col. 6, lines 39-65; col. 7, lines 14-65; col. 10, line 50-col. 11, line 65).

However, Lloyd et al does not specifically disclose the feature of a track and hold circuit having a differential signal input; a bandpass circuit coupled to the differential signal input and the differential mixed signal output.

On the other hand, Williams, from the same field of endeavor, discloses a direct conversion receiver utilizing a sample and hold circuit for sub sampling the input signal. The output of the sample and hold circuit is applied to a sigma-delta loop to provide a high speed low resolution data stream which in turn is applied to a decimator which provides a high precision, low data rate signal having quadrature outputs (fig. 3;ol. 3, lines 49-56). In addition, the output signal from amplifier is sub-sampled by sample and hold circuit clocked by clock CLK1. This allows the frequency of clock signal CLK1 to be conveniently adjusted. By "sub-sampling" signal A, sample and hold circuit 331 provides aliased copies of the original signal (col. 4, lines 18-65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Williams to the system of Lloyd in order to provide a direct conversion receiver utilizing a sample and hold circuit.

Regarding claims 76, 80, 87-88, Lloyd et al discloses a mixer (figs. 3-6; figs. 7-9) where the first signal being within the frequency band; a limiting means for limiting the response of the

track and hold means to a frequency band (col. 6, lines 39-65; col. 7, lines 14-65; col. 10, line 50-col. 11, line 65).

However, Lloyd et al does not specifically disclose the feature of track and hold means for tracking and holding a first signal in response to a second signal.

On the other hand, Williams, from the same field of endeavor, discloses a direct conversion receiver utilizing a sample and hold circuit for sub sampling the input signal. The output of the sample and hold circuit is applied to a sigma-delta loop to provide a high speed low resolution data stream which in turn is applied to a decimator which provides a high precision, low data rate signal having quadrature outputs (fig. 3;ol. 3, lines 49-56). In addition, the output signal from amplifier is sub-sampled by sample and hold circuit clocked by clock CLK1. This allows the frequency of clock signal CLK1 to be conveniently adjusted. By "sub-sampling" signal A, sample and hold circuit 331 provides aliased copies of the original signal (col. 4, lines 18-65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Williams to the system of Lloyd in order to provide a direct conversion receiver utilizing a sample and hold circuit.

Regarding claim 77, Lloyd et al as modified discloses a mixer (figs. 3-6; figs. 7-9) further comprising means for buffering first signal before being applied to the track and hold (col. 3, lines 15-31).

Regarding claim 78, Lloyd et al as modified discloses a mixer (figs. 3-6; figs. 7-9) wherein the track and hold means comprises first and second output signals, the mixer further comprising means for combining the first and second output signals (col. 7, lines 15- col. 8, line 15).

Regarding claim 79, Lloyd et al as modified discloses a mixer (figs. 3-6; figs. 7-9), wherein the limiting means comprises an inductor and capacitor each being coupled to the track and hold means (col. 11, lines 30-66; col. 12, line 44-col. 13, line 48).

Regarding claim 81, Lloyd et al as modified discloses a mixer (figs. 2-3; figs. 9-10), wherein the switch comprises a transistor having a gate coupled to the second signal (col. 9, lines 8-61).

Regarding claim 82, Lloyd et al as modified discloses a mixer (figs. 3-6; figs. 7-9) wherein the transistor filter comprises a source coupled to the first signal (col. 9, lines 12-59).

Regarding claim 83, Lloyd et al as modified discloses a mixer (figs. 3-6; figs. 7-9) wherein the transistor further comprises a drain, and the limiting means comprises a capacitor coupled to the drain (col. 7, lines 14-65; col. 10, line 50-col. 11, line 65).

Regarding claim 84, Lloyd et al as modified discloses a mixer (figs. 3-6; figs. 7-9) wherein the limiting means further comprises an inductor coupled to the source of the transistor (col. 7, lines 14-65; col. 10, line 50-col. 11, line 65).

Regarding claim 85, Lloyd et al as modified discloses a mixer (figs. 3-5; figs. 7-9) wherein the bandpass circuit further comprises an inductor coupled to the source of the transistor (col. 7, lines 14-65; col. 10, line 50-col. 11, line 65).

Regarding claim 86, Lloyd et al as modified discloses a mixer (figs. 3-6; figs. 7-9) wherein the transistor further comprises a drain, and the bandpass circuit comprises a capacitor coupled to the drain (col. 7, lines 14-65; col. 10, line 50-col. 11, line 65).

Regarding claim 89, Lloyd et al as modified discloses a mixer (figs. 3-6; figs. 7-9), wherein the second transistor further comprises a drain coupled to the output of the transistor (col. 7, lines 14-65; col. 10, line 50-col. 11, line 65).

Regarding claim 90, Lloyd et al discloses a mixer (figs. 3-6; figs. 7-9) wherein the limiting means comprises a capacitor coupled to the output of the transistor (col. 7, lines 14-65; col. 10, line 50-col. 11, line 65).

Regarding claim 91, Lloyd et al as modified discloses a mixer (figs. 3-6; figs. 7-9) wherein the second transistor further comprises a source, and the limiting means further comprises an inductor coupled to the source of the second transistor (col. 7, lines 14-65; col. 10, line 50-col. 11, line 65).

Regarding claim 92, Lloyd et al as modified discloses a mixer (figs. 3-6; figs. 7-9) wherein the second transistor further comprises a source, and the limiting means further comprises an inductor coupled to the source of the second transistor (col. 7, lines 14-65; col. 10, line 50-col. 11, line 65).

Regarding claim 93, Lloyd et al as modified discloses a mixer (figs. 3-6; figs. 7- 9), wherein the limiting means comprises a capacitor coupled to the output of the transistor (col. 7, lines 14-65; col. 10, line 50-col. 11, line 65).

Allowable Subject Matter

1. Claims 33-38, 70-75 are allowed.

Allowable Subject Matter

2. Claims 5-13, 15-31,43-59, 62-69 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

3. Applicant's arguments with respect to claims 1-4, 14, 32, 39-42, 61, 76-93 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marceau Milord whose telephone number is 571-272-7853. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F. Urban can be reached on 571-272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. M./

Primary Examiner, Art Unit 2618

/Marceau Milord/

Primary Examiner, Art Unit 2618